US-PAT-NO: 5212541

DOCUMENT-IDENTIFIER: US 5212541 A

TITLE: Contactless, 5V, high speed EPROM/flash EPROM array utilizing cells
programmed using source side injection

---------- KWIC ---------

The cell uses a shared-line source to reduce the cell size. Again, 5V-only
programming is required. Thus, this cell is ideal for use in programmable
logic devices.

US-PAT-NO: 5798548

DOCUMENT-IDENTIFIER: US 5798548 A

TITLE: Semiconductor device having multiple control gates

---------- KWIC ---------

To reduce the occupying area of each memory cell on the substrate 1, two memory
cells 41 (hereinafter indicated by "41a" and "41b" to distinguish those two
from each other) share n type source region 2 (hereinafter indicated by "S").
N type drain regions 2 (hereinafter indicated by "D") of the memory cells 41a
and 41b are connected to an associated one of common bit lines BLa to BLz
(e.g., BLm).

US-PAT-NO: 5548146

DOCUMENT-IDENTIFIER: US 5548146 A

TITLE: Nonvolatile memory device having source and drain of memory cells
integrally formed with data-source lines

---------- KWIC ---------

In order to reduce the size of the memory array, on the other hand, there has
been developed the so-called "contactless array" in which the proprietary
source lines and data lines are not provided unlike the NOR type but in which
common source lines and data lines are formed of buried semiconductor regions
so that they may be shared between adjacent memory cells. The nonvolatile
memory device having such contact array is disclosed, for example, on pp. 311
to 314 of 1991 IEDM (International Electron Devices Meeting) Tech. Dig., 1991
(as will be called as the first reference of the prior art).

In the structure of the memory array thus made, the data line D1 is commonly
used as the source line for the memory cells Q00 to Q20 arranged at the
lefthand side and as the drain line for the memory cells Q01 to Q21 arranged at
the righthand side. Likewise, the data line D2 is commonly used as the source
line for the memory cells Q01 to Q21 arranged at the lefthand side and as the
drain line for the memory cells Q02 to Q22 arranged at the righthand side.
Thus, except the data lines D0 and D3 at the two ends of the memory array, the
data lines D1 and D2 arranged between them can be shared as the source and
drain of the two memory cells adjacent to each other in the

word line direction
so that the memory cell size can be substantially reduced.

US-PAT-NO: 6087229

DOCUMENT-IDENTIFIER: US 6087229 A

TITLE: Composite semiconductor gate dielectrics

---------- KWIC ---------

As semiconductor technology develops, semiconductor device geometries have been reduced. As a result, the various components that make up a semiconductor have been decreased in size. For example, MOS transistor gate widths have been reduced below 0.5 .mu.m to 0.35 .mu.m, 0.25 .mu.m and smaller device sizes are currently being developed. As device sizes decrease, gate dielectric layers in such devices should correspondingly become thinner. For example, in some next generation devices the channel length will be about 0.18 .mu.m and the gate oxide thickness will be about 30 .ANG.. In future generation devices both the channel length and gate oxide thickness will continue to shrink. However, thinner gate dielectrics are more susceptible to failure. Therefore, it is desirable to increase the capability of thin gate dielectrics, commonly oxides, so that they are better able to withstand the high electric fields to which they are subjected in normal operation of smaller semiconductor devices through a process referred to as "hardening".